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LOW POWER DIGITAL DESIGN USING ENERGY-RECOVERY ADIABATIC LOGIC

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Abstract

Increasing demand to improve the system performance especially of portable electronic systems has fueled the necessity of low-power design methodology. In past, area and speed were considerably considered as prime parameters deciding the system performance. Recently, low power design has attracted the attention of many researchers due to increasing demand on small but smart electronic systems. On one side, battery technology is leaping to enhance the battery life while on the other side VLSI researchers are trying to implement number of approaches to minimize power consumption in CMOS chips. Adiabatic logic, which works on the principle of Energy Recovery, is one of the low power approaches for CMOS implementation. In this paper, comparison of energy dissipated and delay of adiabatic logic families viz. Pass-transistor Adiabatic Logic (PAL) and Clocked-CMOS Adiabatic Logic (CAL) with those of conventional CMOS logic. 2:1 multiplexer implementation is presented. The simulation trials were carried out using Cadence ASIC tools with cell bases design approach and 180nm technology. The outcome of this research work will provide guidelines for designing combinational logic circuits for low power and ultra-low power applications.

Keywords: Adiabatic, Energy-Recovery, PAL, CAL.