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DESIGN & VERIFICATION OF QUATERNARY LOGIC CELLS USING THRESHOLD VOLTAGE OF CMOS DEVICES

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Abstract

Design of the binary logic circuits is limited by the requirement of the interconnections and a possible solution can be achieved by using a larger set of signals over a similar chip area, such as multiple-valued logic (MVL) devices. A method to implement quaternary logic cells using CMOS devices is presented in this paper. Quaternary logic cells are designed using enhancement mode MOS transistors. Complement (Quaternary Inverter) analogous to binary INVERTER, NMIN (Quaternary NAND) analogous to binary NAND and NMAX analogous to binary NOR are implemented with voltage mode approach of CMOS technology. Input is applied to three transistors having three different values of threshold voltages. There is a correspondence between values of threshold voltages and logic levels. The features of this type of circuits are small number of transistors and exact transient response.

Keywords: Multiple Valued-Logic, Quaternary