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QUATERNARY MULTILIER ON PROGRAMMABLE LOGIC DEVICE

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Abstract

Design of the binary logic circuits is limited by the requirement of the interconnections and a possible solution can be achieved by using a larger set of signals over a similar chip area, such as multiple-valued logic (MVL) designs. Quaternary logic and number systems are known to offer certain advantages over their binary counter part due to larger information per symbol carried by the former. Common binary arithmetic operations such as addition/subtraction and multiplication suffer from O(n) carry propagation delay where n is the number of digits This paper considers the implementation & verification of quaternary carry-free addition on field-programmable gate arrays (FPGAs). Considering constant delay model the results for multi quaternary digit with consistent performance are verified. This paper is in continuation with earlier work presented[1].

Keywords: Quaternary signed digit, Carry Propagation, FPGA.