DIFFERENT APPROACHES OF PARTITIONING TECHNIQUES TESTED FOR OPTIMIZATION, IN VLSI DESIGN

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Abstract

Various applications of VLSI circuits in high-performance computing, telecommunications, and consumer electronics has been expanding progressively, and at a very hasty pace. There are various algorithms for the partitioning techniques already available. This paper deals with some of the new algorithms worked on the techniques. First one is the Memetic algorithms (MA) are population based heuristic search approaches for combinatorial optimization problems based on cultural evolution. Next is Neuro-memetic model which makes it *possible to predict* the sub-circuit from circuit with minimum interconnections between them. Another new model for partitioning a circuit is using DBSCAN and fuzzy ARTMAP neural network. The last work in this paper is about two clustering algorithms Nearest Neighbor (NNA) and Partitoning Around Medoids (PAM) clustering. The results and performance of these algorithms tested, is been presented here.