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A NOVEL FAULT TOLERANT DESIGN AND AN ALGORITHM FOR TOLERATING FAULTS IN DIGITAL CIRCUITS

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Abstract

This paper proposes a novel fault tolerant algorithm for tolerating stuck-at-faults at in digital circuits. A stuck-at-fault may adversely affect on the functionality of the user implemented design. A novel fault tolerant design based on hardware redundancy (replication) is presented here for single fault model to tolerate transient as well as permanent faults. The design is also suitable to be used for highly dependable systems implemented by means of Field Programmable Gate Arrays (FPGAs) at RTL level. This approach offers the possibility of using larger and more cost effective devices that contain interconnect defects without compromising on performance or configurability. The algorithm presented here demonstrates the fault tolerance capability of the design and is implemented for a full adder circuit but can be generalized for any other digital circuit. Using exhaustive testing the functioning of all the three full adders can be easily verified. In case of occurrence of stuck-at-faults; the circuit will configure itself to select the other fault free outputs. We have evaluated our novel fault toleranttechnique (NFT) in five different circuits: full adder, encoder, counter, shift register and microprocessor. The proposed design approach scales well to larger digital circuits also and does not require fault detection. We have also presented and compared the results of triple modular redundancy (TMR) method with our technique .All possible faults are tested by injecting the faults using a multiplexer.

Keywords: Fault tolerance, fault injection, field programmable gate arrays (FPGA), reconfiguration, triple modular redundancy (TMR), novel fault tolerant technique (NFT).