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VLSI IMPLEMENTATION OF FIR FILTER USING PROCESSOR

PRASHANTMANI, JUNAID KHAN AND R. P. MAHAPATRA

Abstract

Finite impulse response (FIR) filter is the key functional block in the field of digital signal processing. A number of implementations can be found in the public literatures, either by software or hardware solutions. The proposed design is trying to answer the question on whether a solution can be achieved with minimal cost of hardware and software, and how is its performance. In the VLSI implementation, the hardware complexity of the FIR filter is directly proportional to the tap length and the bit-width of input signal. To reduce the hardware cost, this can be solved with iteration calculations by software; therefore, a co-design of hardware and software may produce cost-efficient FIR filters. The key design concept is to build a processor for software processing with minimum hardware resources, without sacrificing the performance of original FIR filter. The proposed design methodology can be considered as an intellectual property (IP) design for FIR filters in system-on-a chip (SOC) environment.

Keyword : FIR,JBS, Vonneumann, ALU, CPU, FPGA