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HIGH PERFORMANCE TAM CONTROLLER AND WRAPPER DESIGN FOR EMBEDDED CORES

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Abstract

IEEE 1500 is a standard under development which intends to amend ease of test reuse and test integration with respect to the core-based system-on-chip(SoC). The subject paper proposes evolving the wrapper cell design for SoC testing used in the IEEE 1500 standard for digital embedded cores. The digital cores used in the study were constructed from ISCAS 85 combinational and ISCAS 89 sequential benchmark circuits. The wrapper that separates the core under test from other cores is assumed to be IEEE 1500- compliant. The test access mechanism plays an important role in transporting the test patterns to the desired core and the core responses to the output pin of the SoC. The faults were injected using a fault simulator that generates tests for the core. The cores and test access mechanism were described using VHDL. The test access mechanism (TAM) provides the connection between the test sources, cores, and test sinks, which is crucial in any SoC design. The outcome was the fault coverage of all the cores being tested. Area overhead and power consumption are taken into account in our scheme. Experiment results based on a sample SoC are reported, showing the effectiveness of the proposed approach in terms of area overhead and power consumption.

Keywords : Built-in self-testing (BIST), embedded cores-based system-on-a-chip (SoC), sequential circuits, test access mechanism (TAM), test pattern generator (TPG), VHDL, wrapper.