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ANALYSIS OF MULTILEVEL INVERTER TOPOLOGIES AND OUTPUT VOLTAGE HARMONIC REDUCTION

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Abstract

This paper concentrates on studying the analysis of output voltage waveforms of cascade H-bridge multilevel inverter and flying capacitor type multilevel inverter topologies with various switching schemes and it also deals with the minimization of the total harmonic distortion(THD) when controlling a multilevel inverter to act as a static var compensator. Here, the multilevel inverter's power electronic devices are switched at the fundamental frequency while eliminating the lower order harmonics. The multilevel inverter is operated in an optimum amplitude modulation index regime so that the output voltage total harmonic distortion (THD) is kept to a minimum. The cascaded H-bridges and the flying capacitor multilevel inverter topologies are compared for THD reduction. The cascade multilevel inverter (CMLI) is one of the most important topology in the family of multilevel inverters. It requires least number of components when compared to diode-clamped and flying capacitor type multilevel inverters (FCMLI). It has modular structure with simple switching strategy and occupies less space. Simulation results also reveal that the cascaded H-bridge inverter topology is the better choice for reduction of THD.

Keywords: Amplitude modulation index, Multilevel inverter, Static var compensator, THD.