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OPTIMIZATION OF POWER AND AREA IN SELF-CHECKING CARRY-SELECT ADDER DESIGN BASED ON TWO-RAIL ENCODING

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Abstract

Arithmetic operations are frequently used in many VLSI-based systems. The design of faster and highly reliable adders is of major importance in such systems. Carry-select adders are one of the faster types of adders. This paper proposes a scheme that encodes the sum of bits using two rail codes. Self-Checking Checkers checks the encoded sum bits. The multiplexers used in the adder are also totally self-checking. This scheme is illustrated with the implementation of a 2-bit Carry select adder that can detect all single stuck-at faults on line. The detection of double faults is not guaranteed. Adders of arbitrary size can be constructed by cascading the appropriate number of such 2-bit adders. A range of adders from 4 to 32 bits is designed using this approach employing a 0.12µm CMOS technology. The transistor overhead in implementing these self-checking adders varies from 14.27 % to 19.67 %, and the area overhead is 31.2 % Compared to the adders with out built-in self-checking capability.

Keywords: CMOS, Self-Checking, Low Power, Full-Adder