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DESIGN OF POWER MANAGEMENT PROCESSOR/CONTROLLER FOR EMBEDDED APPLICATION

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Abstract

Minimization of power consumption in portable and battery powered embedded systems has become an important aspect of processor and system design with the demand for portable products. Hence power has become an important aspect in the design of general purpose processors. This project explores how design tradeoffs affect the power and performance of the processor. Scaling the technology is an attractive way to improve the energy efficiency of the processor. In a scaled technology a processor would dissipate less power for the same performance or higher performance for the same power. Basically there are two scaling techniques Dynamic voltage scaling and Dynamic frequency scaling. In our project we are mainly implementing Dynamic frequency scaling. We consider 2 or more peripherals connected to the system called as power management module. Depending on the request sent by the two peripherals low or high frequency will be given to the peripherals. In case no request is made by both peripherals power management module will wait for 10 clock cycles, then peripherals will be made to go to sleep mode. Once the request is received, the controller module wakes up the peripheral with interrupt after it receives the request. A provision for voltage has been made in the project and the voltage values implemented are 3.3Volts and 1.2 Volts. We also use 0 or very low for sleep mode. The frequency values used are f/2, f/4, f/8 and f/16 where f is the input clock frequency.

Keywords: Power Management Controller, Dynamic Voltage Scaling and Frequency Scaling, Sleep mode, Power Optimization