International J. of Engg. Research & Indu. Appls. (IJERIA).
ISSN 0974-1518, Vol. 3, No. III (August 2010), pp. 403-412

DESIGN AND ANALYSIS OF VITERBI AND ADAPTIVE VITERBI DECODER

N. D. BOBBY, S. K. SRIVATSA AND LAL KISHORE

Abstract

The use of error-correcting convolutional codes provides a proven mechanism to limit the effects of noise in digital data transmission. Although hardware implementations of decoding algorithms, such as the Viterbi algorithm, have shown good noise tolerance for error correcting codes, these implementations require an exponential increase in VLSI area and power consumption to achieve increased decoding accuracy. To achieve reduced decoder power consumption, in this paper we provide a comprehensive comparison of Viterbi decoder and adaptive Viterbi decoder. We have examined and implemented decoders based on the reduced-complexity Adaptive Viterbi algorithm (AVA). In order to minimize power consumption and minimize BER, experimental calculations indicate that the use of Adaptive Viterbi decoder leads to a reduction in decoder power consumption over a Viterbi decoder field programmable gate array (FPGA) implementation with no loss of decode accuracy.

Keywords: VLSI, Viterbi decoding, FPGA, Adaptive Viterbi decoding.