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VLSI BASED MIXED-RADIX 4-2 BUTTERFLY FFT FOR WIRELESS COMMUNICATION

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Abstract

The fast Fourier transform (FFT) and inverse FFT (IFFT) operations are used as the modulation/demodulation kernel in the OFDM systems, and the sizes of FFT/IFFT operations are varied in different applications of OFDM systems. The modified Mixed Radix Butterfly FFT with bit reversal for the output sequence derived by index decomposition technique is our suggested VLSI system architecture to design the prototype FFT/IFFT processor for OFDM systems. The analysis of several FFT algorithms such as radix-2, radix-4 and split radix were designed using VHDL. The results show that the proposed processor architecture can greatly save the area cost while keeping a high-speed processing speed, which may be attractive for many real-time systems.

Keywords : OFDM, FFT/IFFT, VLSI, VHDL, Mixed Radix with bit reversal.

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