International J. of Engg. Research & Indu. Appls. (IJERIA). ISSN 0974-1518, Vol.4, No. II (May 2011), pp 219-228

VLSI IMPLEMENTATION OF 2- DIMENSIONAL DISCRETE WAVELET TRANSFORMS

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Abstract

This paper presents a VLSI implementation of discrete wavelet transform (DWT) for image compression. This can be used for both lossy and lossless compression. In order to reduce complexities of the design, linear algebra view of DWT and IDWT has been used in this paper. This architecture can be used for image compression. The architecture is simple, modular, and cascadable for computation of one, or multi-dimensional DWT. It comprises of four basic units: input delay, filter, register bank, and control unit. The proposed architecture is systolic in nature and performs both high-pass and low-pass coefficient calculations with only one set of multipliers. In addition, it requires a small on-chip interface circuitry for interconnection to a standard communication bus.

Keywords: Discrete wavelet transforms (DWT), image compression, thresholding, VLSI design.

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