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ON CHIP CROSSTALK NOISE EFFECTS MEASUREMENT AND ANALYSIS FOR VLSI CIRCUITS

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Abstract

This paper presents an approach for the analysis and the experimental evaluation of crosstalk effects. Crosstalk can result in significant delay variations as well as signal integrity problems in modern day CMOS circuit design, minimizing the power dissipation and the delay due to cross–talk in data propagation has been of much great interest to the research community. An important component of power consumption and delay due to cross-talk in processors is the transmission of data through high capacitance system-level buses. Crosstalk induced delay and power consumption have become a major determinant of the system performance. Reducing crosstalk can greatly boost the system performance. Bus encoding Schemes can achieve the same amount of bus delay improvement as passive shielding with a much lower area overhead. Several techniques like inserting the buffers, bus encoding with and without memory, etc. are available for mitigating the crosstalk. The technique we followed is memoryless bus encoding, because it is less complex compared to other techniques. We designed a CODEC and implemented, which uses very small area, consumes small amount of power and exhibits very small delay from input to output.

Keywords : System on chip, network on chip, deep submicron, chip level multiprocessing, crosstalk