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RECONFIGURABLE MULTIPLIER ON FIR FILTER FOR SDR RECEIVER

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Abstract

The continually increasing integration density of integrated circuit, with astronomical increase in fabrication cost and enormous time to market portrays important paradigm shift in next generation System –on-Chip (SoC) design. This leads more programmable designs that can spin a wide range of applications. Hence there is a trend away from the fixed SoC to highly flexible SoC with improved time to market. The reconfigurability in SoC can be achieved either by the Programmable gate arrays [FPGA] and/or through Programmable interconnect. The emergence of static memory based FPGA that are capable of being dynamically reconfigured i.e. partially programmable during run time has been a driving force for flexible architecture. Software defined radios (SDRs) offer a programmable and dynamically reconfigurable method of reusing hardware to implement the physical layer processing of multiple communications systems. An SDR can dynamically change protocols and update communications systems over the air as a service provider allows. The most computationally demanding block of a software defined radio (SDR) receiver is the channelizer which operates at the highest sampling rate. Reconfigurability and low complexity are the two key requirements of the SDR channelizers in Programmable Device. Two new reconfigurable architectures of low complexity finite impulse response (FIR) filters for channelizes are proposed in this paper. Our methods are based on the binary common sub expression elimination (BCSE) algorithm.