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ALGORITHMS FOR DIGITAL MULTIPLIER AND SQUARE ARCHITECTURE BASED ON VEDIC MATHEMATICS

S. M. KHAIRNAR[1], S. ARUNACHALAM[2] AND B. S. DESALE[3]
[1] Professor and Head, Department of Engineering Sciences,
Maharashtra Academy of Engineering, Alandi, Pune - 411 105, India.
[2] Associate Professor, Department of Mathematics,
Rizvi College of Arts, Science & Commerce, Bandra (West), Mumbai – 400 050, India.
[3] Department of Mathematics, North Maharashtra University, Jalgaon – 425 001, India.

Abstract

Digital Signal Processors (DSP) are very important in various engineering disciplines. Fast multiplication is very important in DSP for Convolution, Fourier Transforms etc. Highly efficient arithmetic operations are necessary to achieve the desired performance in Digital Image Processing applications. Since multiplication is the core computing process of most DSP algorithms, so there is a need for high speed multiplier. Multiplier architecture algorithm and a reduced-bit multiplication algorithm based on the ancient Indian vedic multiplication formula is proposed in this paper. The work mainly focuses on speed of the multiplication operations of multipliers by reducing the number of bits to be multiplied. The framework of the proposed algorithm is taken from mathematical algorithms given in vedas and is further optimized by use of general arithmetic operations such as expansion and bit-shifting to take advantage of bit-reduction multiplication.

Keywords: Vedic algorithm, Urdhva Tiryakbhyam sutra, Nikhilam sutra, Multiplier architecture, Reduced-bit.