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DESIGN OF LDPC ENCODER AND DECODER CIRCUIT OF OFDM

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Abstract

In this paper we have design a wave pipelined LDPC decoder architecture and their comparison with pipelined, non-pipelined and wave pipelined architectures, the results shows that the wave pipelined method LDPC decoder architecture will take low area and minimal power when compared with other pipelined architectures. The hardware implementation was targeted on FPGA, because it has the advantage of flexibility over traditional ASIC implementation. Due to their near Shannon limit performance and inherently parallelizable decoding scheme, low-density parity-check (LDPC) codes. have been extensively investigated in research and practical applications. Recently, LDPC codes have been considered for many industrial standards of next generation communication systems such as DVB-S2, WLAN (802.11.n), WiMAX (802.16e), and 10GBaseT (802.3an). For high throughput applications, the decoding parallelism is usually very high. Hence, a complex interconnect network is required which consumes a significant amount of silicon area and power.