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THE MULTI-CORE BOTTLENECK

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Abstract

The present day Multi-core Processors a.k.a., Chip Multi Processors (CMPs) fail to meet the expectations of the End users. This is in compliance with the Amdahl's law that predicts the maximum number of paralleizable Cores. This state of the processor is termed as "The Multi-core Bottleneck". We propose an alternate Neuron Processor design, which resembles the present day CMP design and resolves utilization of cores further to higher limits. As per the literature available Von Neumann also thought off some what a similar design during his stay at the Yale University in 1956. In this paper we identify the performance Bottleneck with increase in the number of cores in the present day Chip Multi Processors. This is very similar to the situation of the Von Neumann bottleneck with higher processor speeds, prior to the inclusion of Cache Memory to the processor architecture. Further we suggest an alternate architecture so as to improve the speed-up to the extent possible at the present day's silicon technology by utilizing the full bandwidth of the bus connecting the cores to the front end in a CMP.

Keywords : Chip Multi Processor, Von Neumann architecture, Amdahl's Law, Cache Memory, Biological Neuron, Artificial Neuron.