

DESIGN OF LOOP FILTER FOR HIGH PERFORMANCE PHASE LOCKED LOOP USING 0.18 μM CMOS TECHNOLOGY

R. H. TALWEKAR AND S. S. LIMAYE

Abstract

This paper presents a simple architecture of loop filter and describes the dynamics of the loop filter in the PLL. An on chip loop filter is designed for PLL and simulated in 0.18 μM CMOS Technology. A proposed architecture of loop filter has designed and simulated by T Spice. A second order low pass filter needed to supply the voltage required to control the VCO in the PLL has been designed with less die area, high performance capability and low power dissipation. The simulated PLL provides the loop parameters almost independent of divider factor and decreases the capacitance to $1/20^{\text{th}}$ of conventional PLL. The design of 2.4 GHz complementary metal oxide semiconductor (CMOS) phase locked loop(PLL) targeting orthogonal frequency division multiplexing (OFDM) application has been described . The proposed PLL filter has been designed with 1.8V supply and 0.18 μM CMOS Technology. The details of the dynamics of the loop filter is described and simulated for better results with less non-ideality in the voltage controlled oscillator (VCO) input response. A 100 μA charge pump has been used to force the current pulses to low pass filter. The specific low pass filter designed and described here, is very useful to avoid the disturbance to VCO. This is achieved by properly designed loop filter which gives very low ripple to VCO.

Keywords: Phase locked loop, complementary metal oxide semiconductor, orthogonal frequency division multiplexing voltage controlled oscillator.