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A BUS ENCODING TO REDUCE CROSSTALK NOISE EFFECT IN SYSTEM ON CHIP

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Abstract

This paper proposes a new bus coding scheme for reducing the crosstalk in soc. As circuit geometries become smaller, wire interconnections become closer together and taller, thus increasing the cross-coupling capacitance between nets. At the same time, parasitic capacitance to the substrate becomes less as interconnections become narrower, and cell delays are reduced as transistors become smaller. With circuit geometries at 0.25 micron and above, substrate capacitance is usually the dominant effect. However, with geometries at 0.18 micron and below, the coupling capacitance between nets becomes significant, making crosstalk analysis increasingly important for accurate timing analysis. We show experimentally that the proposed codes allow reducing crosstalk delay by at least 14% based on available data.

Keywords : Crosstalk, Encoding, SOC, parasitic, coupling Capacitance, micron.