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SIMULATION OF SECOND-ORDER ANALOG PHASE-LOCKED LOOP FOR STUDYING THE PULL-IN TIME

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Abstract

This work presents a method for simulating second-order analog Phase Locked Loops (PLL) in time domain for studying the pull-in time with dynamic limits. A basic PLL system may consist of a multiplier used as phase detector (PD), a passive loop filter (LF) and a voltage controlled oscillator (VCO). The method uses the phase error process to study the pull-in time with dynamic limits such as lock-in limit, pull-in limit. The method is mainly based on companion network modeling of the loop filter and mathematical modeling for VCO and the multiplier. The complete simulation program for the PLL system is written in Turbo C language. The MATLAB program is used for graphical analysis of data generated by the simulation program. The dynamic limits such as lock-in and pull-in are observed. The values of dynamic limits known from literature of PLL are compared and verified with the simulated values.

Keywords : Phase-Locked Loop, Phase error process, Lock-in, Pull-in, Pull-in time, Companion network model.