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DESIGN A LOW POWER AND AREA EFFICIENT NEW RECONFIGURABLE FIR FILTER FOR DSP APPLICATIONS

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Abstract

This paper presents an architectural approach to the design of Low power and area Reconfigurable finite impulse response (FIR) filter. FIR digital filters are used in DSP by the virtue of its, linear phase, fewer finite precision error, stability and efficient implementation. The proposed architectures offer Low power and area reductions and compared to the best existing reconfigurable FIR filter implementations in the literature and the proposed architectures have been implemented and tested on Spartan-3 xc3s200-5pq208 field-programmable gate array (FPGA) and synthesized.

Keywords : Channelizer, FIR filter, high speed filter, Reconfigurability